Run IIb Event Builder upgrade









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Motivation Scope **Progress End game & Installation**

CDF Run IIb TDR

Trigger	Rates at $4 \times 10^{32} \text{ cm}^{-2} \text{s}^{-1}$		
	L1	L2	L3
e/μ	$2,327~\mathrm{Hz}$	$250~\mathrm{Hz}$	$22~\mathrm{Hz}$
ν	$4,401~\mathrm{Hz}$	$130~\mathrm{Hz}$	9 Hz
calibration	2,940 Hz	117 Hz	16 Hz
Total	$9,668 \; \mathrm{Hz}$	497 Hz	$47~\mathrm{Hz}$

Table 6.1: Summary of trigger rates for Higgs search triggers at $\mathcal{L} = 4 \times 10^{32} \text{ cm}^{-2} \text{s}^{-1}$. These triggers are important for many other high- p_T physics analyses.

Trigger	$\sigma_{L1}(\mathrm{nb})$	$\sigma_{L2}(\mathrm{nb})$	$\sigma_{L3}(\mathrm{nb})$
High- p_T jets	19,000	60	17
$t\bar{t}$ (all hadronic)	(overlap)	50	5
$ auar{ au}$	5,000	50	4
$ \not\!\!E_T + \tau $	(overlap)	50	$\overline{4}$
High- E_T photons	13,500	110	21
di,tri-leptons	1,000	190	45
Total	38,500	660	96
Total rate	$15,400~\mathrm{Hz}$	264 Hz	38 Hz

Table 6.2: Summary of triggers necessary for the CDF Run IIb high- p_T physics program. The estimated rates shown are for an instantaneous luminosity of $\mathcal{L} = 4 \times 10^{32} \text{ cm}^{-2} \text{s}^{-1}$.

Specs

Runlla

Rate: 300Hz

Event size: 250kB

Throughput: 75MB/s

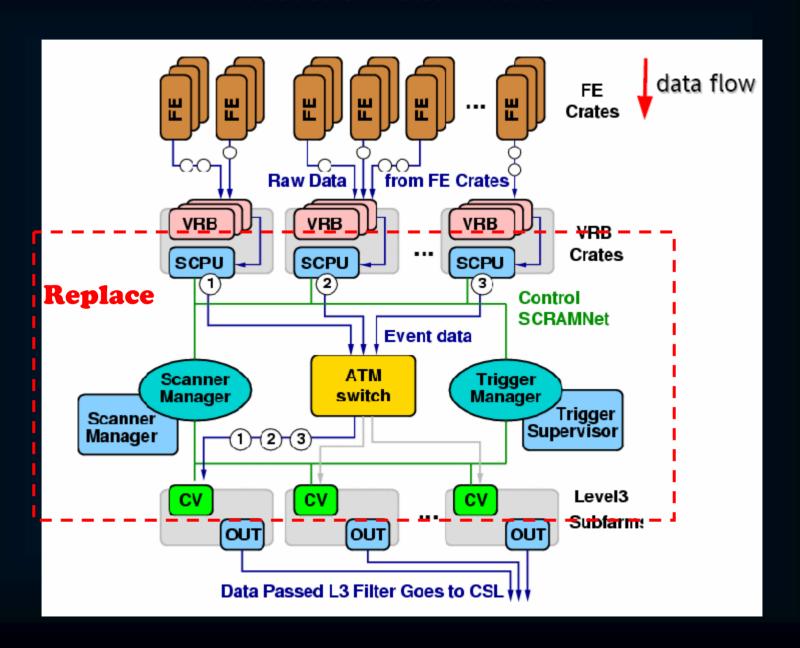
Run IIb

1kHz

500kB

500MB/s

Current Event Builder



Run IIb Event Builder Upgrade

Milestones



Sept 2003



switch technology choice, place order for final system switch arrival of final system switch, install test stand

Cisco GbE switch selected and installed





"Complete overkill"

Run Ilb Event Builder Upgrade

Milestones

Sept 2003	switch technology choice, place order for final system switch
Jan 2004	arrival of final system switch, install test stand
May 2004	SCPU choice, place order for final system SCPUs, complete code design
Sept 2004	arrival of final system SCPUs, code skeleton complete, start of testing during Summer shutdown

Single board computers to read out VME crates

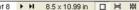
20 boards ordered and received

Read/send rate of 36-40 MB/s over VME backplane achieved, exceeding 30 MB/s spec



VMIVME-7805 Intel® Pentium® 4 Processor-M Based VMEbus Single-Board Computer

- Pentium[®] 4 Processor-M µFCPGA socket processor-based single-board computer (SBC) with 400 MHz system bus
- Special features for embedded applications include:
- Up to 1 Gbyte bootable flash on secondary IDE (optional)
 Two 16-bit and two 32-bit programmable timers
- 32 Kbyte of nonvolatile SRAN
- Software-selectable watchdog timer with reset
- Remote Ethernet booting
- PMC expansion site (IEEE-P1386 common mezzanine card standard, 5 V)
- VME64 modes supported: A32/A24/D32/D16/D08(E0)/MBLT64/BLT32
- VMEbus interrupt handler, interrupter and system controller
- Includes real-time endian conversion hardware for little-endian and big-endian data interfacing (patent no. 6.032,212)
- Enhanced bus error handling
- Passive heat si
- Standard features for embedded applications include:
 A 200 CH Partition 4 Page 14 April 540 KH.
- Up to 2.20 GHz Pentium 4 Processor-M with 512 Kbyte advanced transfer cache
- Up to 1 Gbyte PC2100 DDR SDRAM using two SODIMMs
- Internal SVGA and DVI controller
- 400 MHz system bus via Intel[®] 852GM chipset
- One Ethernet controller supporting 10BaseT and 100BaseTX interfaces
 One Ethernet controller supporting 10BaseT, 100BaseTX and 1000BaseT
- interfaces







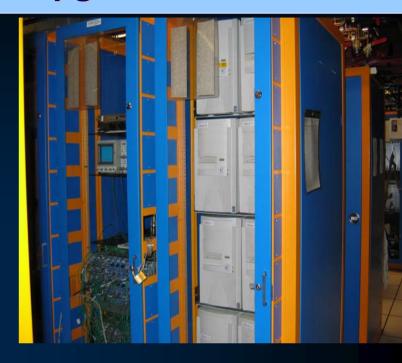
Additional features within the Intel NetBurst mico-architecture include advanced dynamic execution.



Run Ilb Event Builder Upgrade

All hardware now in hand Gigabit switch (1) new SCPUs (20)

Additional test stand hardware 16 PCs acting as "Level 3" Cisco 3750 switch



We are also upgrading Level 3 Converter Nodes (16 nodes) and Output Nodes (8 nodes)

Purchase order is being placed

Run Ilb Event Builder Upgrade

Summer 2004 Shutdown Milestones

```
Oct 1 2004
            Small test
                   1 new SCPU
                   dummy Level 3
                   limited Run Control interface
                   no interface to Trigger Manager
Nov 1 2004
              Medium test
                   several new SCPUs
                   dummy Level 3
                   functional Run Control interface
                   functional Trigger Manager interface
Dec 1 2004
              Large test
                   all SCPUs
                   full Level 3

✓ full Run Control interface

                   full Trigger Manager interface
```

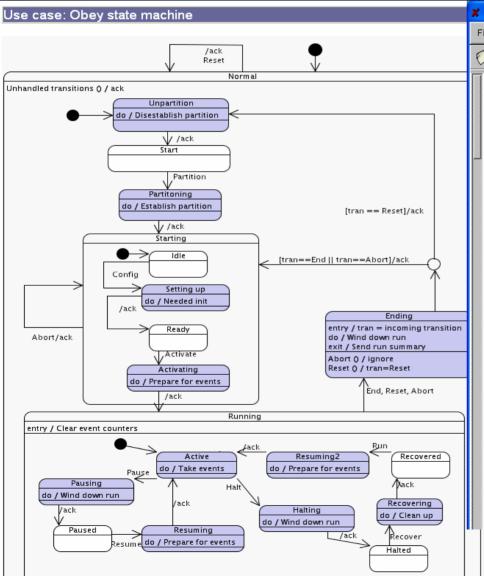
Extensive code design

(http://mit.fnal.gov/~klute/design/)



Real implementation

(https://www-cdfonline.fnal.gov/cgibin/cvsweb.cgi/cdfevb2/)



```
emacs@b0evb2gate.fnal.gov
 File Edit Options Buffers Tools C++ Help
    // Markus Klute, klute@fnal.gov
    // created: Sun May 09, 2004
   // $Id: StateMachine.cc, v 1.20 2004/11/17 03:25:28 klute Exp $
   #include <scpu/StateMachine.hh>
   #include <scpu/StateMachineDriver.hh>
   #include <scpu/Messages.hh>
   #include <evb/MainTrans.hh>
   #include <evb/AceUtil.hh>
   #include <evb/Message.hh>
   using evb::Message;
   #include <boost/shared ptr.hpp>
   using boost::shared ptr;
   namespace scpu {
     const QEvent StateMachine::AckSetupVrb EVENT = { AckSetupVrb SIG,
     const QEvent StateMachine::AckPrepareL3 EVENT = { AckPrepareL3 SIG,
                                                                           0, 0 };
     const QEvent StateMachine::Configuration EVENT = { Configuration SIG
                                                                           0, 0 };
     const QEvent StateMachine::AckConfigVrb EVENT = { AckConfigVrb SIG,
                                                                           0, 0 };
                                                                           0, 0 };
     const QEvent StateMachine::AckConfiqRun EVENT = { AckConfiqRun SIG,
     const QEvent StateMachine::AckVrbReset EVENT = { AckVrbReset SIG,
                                                                           0, 0 };
     const QEvent StateMachine::Setup EVENT
                                                                           0, 0 };
                                                    = { Setup SIG,
      // *** Waiting for EvbVrbList.
      QSTATE StateMachine::partitioning(QEvent const *e)
        switch(e->sig)
         case Q ENTRY SIG:
             ACE DEBUG ((LM DEBUG, "(%P/%t) StateMachine : partitioning-ENTRY, \n"));
         case Q EXIT SIG:
             ACE DEBUG ((LM DEBUG, "(%P/%t) StateMachine : partitioning-EXIT, \n"));
             return 0:
         case Done SIG:
             ACE DEBUG ((LM DEBUG, "(%P/%t) StateMachine : partitioning-Done.\n"));
             Q TRAN(&StateMachine::starting);
             shared_ptr<const Message> msg(new evb::AckPartition());
             driver() send(msq)
```

Run Ilb Event Builder Upgrade

Milestones

V	Sept 2003	switch technology choice, place order for final system switch
\	Jan 2004	arrival of final system switch, install test stand
	May 2004	SCPU choice,
V		place order for final system SCPUs, complete code design
	Sept 2004	arrival of final system SCPUs, code skeleton complete,
		start of testing during Summer shutdown
V	Jan 2005	completion of Shutdown testing
	May 2005	code complete, system ready for installation
	Sept 2005	Run Ilb Event Builder installed

Study of the Event Size and the Performance of the Run IIb Event Builder System.

CDF-7327

Markus Klute

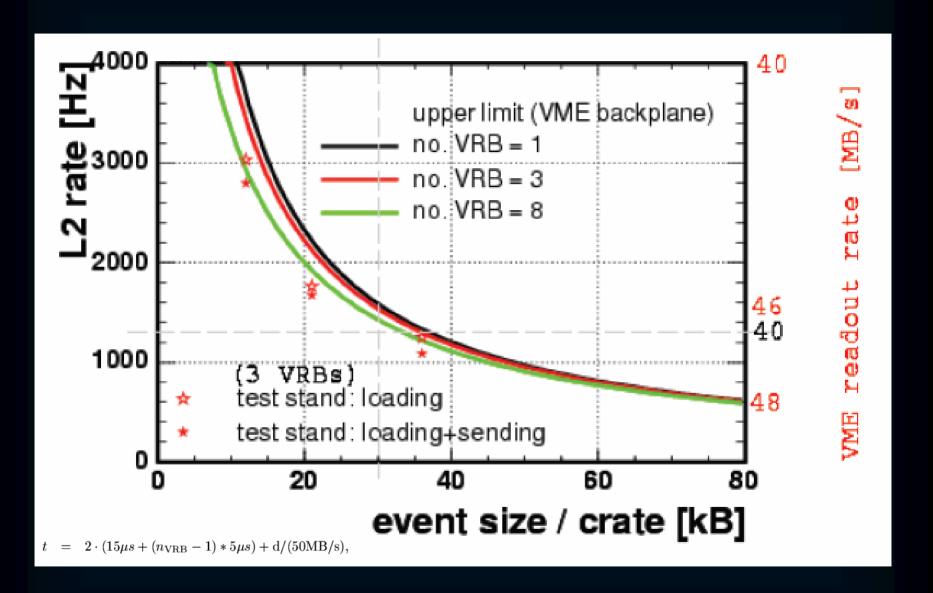
Massachusetts Institute of Technology

December 13, 2004

This note describes an analysis of the event fragment size in Event Builder VME crates and the performance of the Run IIb event builder system. A recommendation is given to increase the number of VME crates in order accommodate the estimated event size at the projected Tevatron peak luminosity.

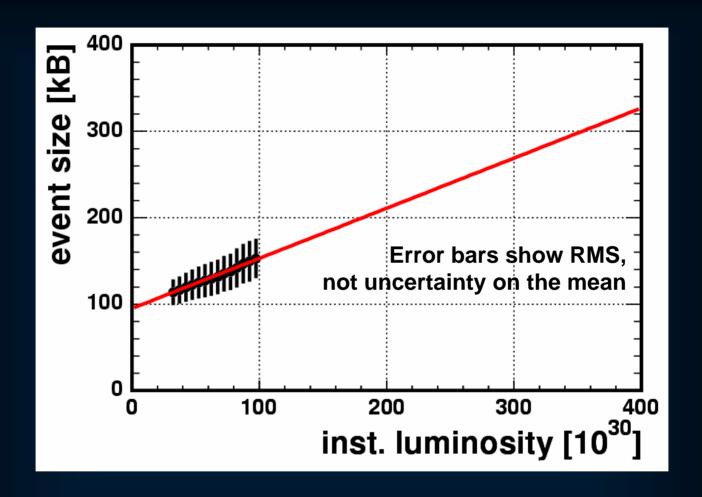
Our bandwidth limit will be the VME backplane

Achiev[ed/able] rates



(code currently in flux)

Projected Event Size through DAQ (sans Silicon) VRB crates



 $(300 \text{ kB} / 6 \text{ DAQ crates}) / (30 \text{ MB/sec VME readout}) = 1.7 \text{ ms} \rightarrow 600 \text{ Hz}$ $(300 \text{ kB} / 12 \text{ DAQ crates}) / (30 \text{ MB/sec VME readout}) = 0.8 \text{ ms} \rightarrow 1.2 \text{ kHz}$

We are therefore adding 6 extra DAQ VRB crates

Cost: $\approx 40 \text{ k}$ \$

6 VMIC 7805 boards at \$2700 each = 16 k\$

4 Rittal VIPA crates at \$4000 each = 16 k\$

Misc infrastructure (power cables) ~ 10 k\$

We are also rearranging Silicon VRB crates to balance load

Report of the December 17, 2004 Run2b Event Builder Upgrade Review

William Badgett, Guillelmo Gomez-Ceballos, Steve Nahn, Jim Patrick, Mel Shochet

Run 2b Event Builder Upgrade Review Committee

Abstract

This is a report on the findings of the Review committee for the Run 2B Event Builder based on the presentations of the review of December 17, 2004.

Contents

1	Introduction							
2	General							
3	Comments and Recommendations from the committee 3.1 Throughput calculations							
	3.2 Error Handling and Efficiency of Operation							
	3.4 Additional Crates							
4	Summary							

Committee recommendations:

1. Optimize code

We are concentrating on optimization while completing the full functionality of the system. Last week we eliminated two of two time-consuming copies of data in memory, and we are beginning to bundle messages for increased speed.

2. Error handling

We are adding dumps of event information when an error is seen. Our design will handle most errors with a "HRR" (CDF jargon), which costs a few seconds.

Committee recommendations:

3. Commissioning and operations

We have added hardware to the VRB crates so that switching between new and old systems costs ~ 15 min

We will be conducting tests with the CDF DAQ this Spring, using our test stand to ensure good use of this time

New personnel (2 graduate students, 1 postdoc) are being brought on board to learn system, carry pager

4. Additional VRB crates

We are adding 6 additional DAQ VRB crates to the system, and are rearranging Silicon VRBs.

Summary (1 of 2)

- All hardware is in hand
- Significant progress in code development
- Desired rates have been demonstrated
- Combination of
 - current CDF event builder expertise
 - existing DO event builder expertise
 - young blood

has proven valuable

(Steve Tether)

(Ron Rechenmacher)

(Markus Klute)

 Thanks to many involved in the CDF DAQ and operations Frank, JJ, Bill, Steve, Peter, Pat, Cheng-Ju, Rob, Dervin, and others

Summary (2 of 2)

- We are on target for completion by May-Aug 2005
- Possibility exists to install before Summer Shutdown 2005
- Quick swap between old and new systems enables commissioning of new system during hours without beam over the next few months
- We will use (occasional) access to the CDF DAQ to do this commissioning

Looking forward to a tripling of rate and sextupling of throughput into CDF Level 3